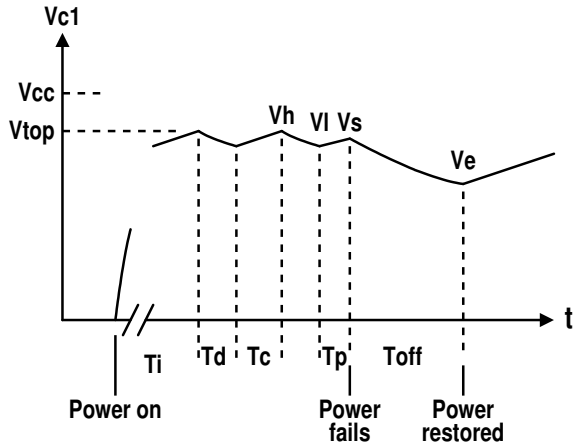


R1, R2 protect C1 from GPIO upsets  
 C1, R2 control RC timing  
 R3 pulls CHARGE low when off  
 C2 filter, ADC buffer (optional)

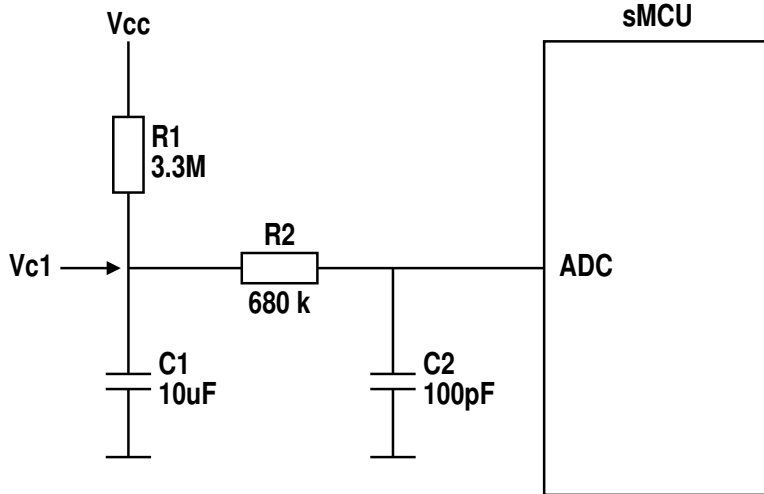
Phase	ADC	CHARGE
Charge	H	H
Discharge	Z	Z
Sample	ADC	Z



$V_{cc}$  = supply voltage (3.3 V)  
 $V_{top}$  = end of charge, 90% of  $V_{cc}$  (?)  
 $V_{min}$  =  $V_l$  goal, 90% of  $V_{top}$  (?)  
 $V_h$  = measured high voltage  
 $V_l$  = measured low voltage  
 $V_s$  = measured/estimated start voltage  
 $V_s = f(V_h \text{ or } V_l, T_p, T)$   
 $V_e$  = measured end voltage

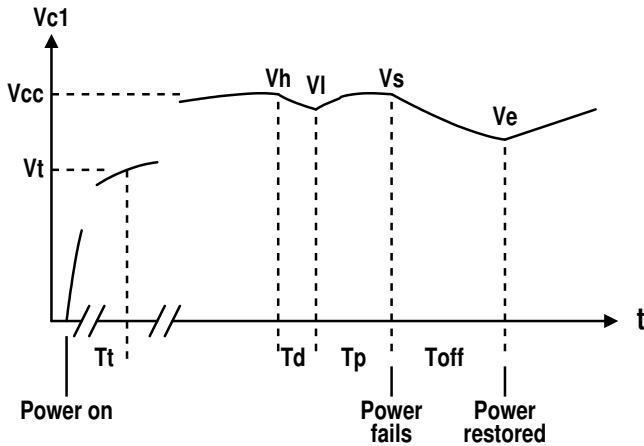
$T_i$  = initial charge time  
 determined by reaching  $V_{top}$   
 $T_d$  = discharge time,  $f(V_{top}, V_{min}, T)$   
 $T_c$  = charge time,  $f(V_{top}, V_l, T)$   
 $T_p$  = partial charge/discharge time  
 $T_{off}$  = calculated off time,  $f(V_s, V_e, T)$   
 $T$  = timing coefficient,  $f(V_{top}, T_i)$   
 (needs continuous recalibration)

Design proposed by Joerg Reisenweber



C1, R1 control RC timing  
 R2 protects C1 from GPIO upsets  
 C2 filter, ADC buffer (optional)

Phase	ADC
Discharge	L
Idle	Z
Sample	ADC
Fast charge	H

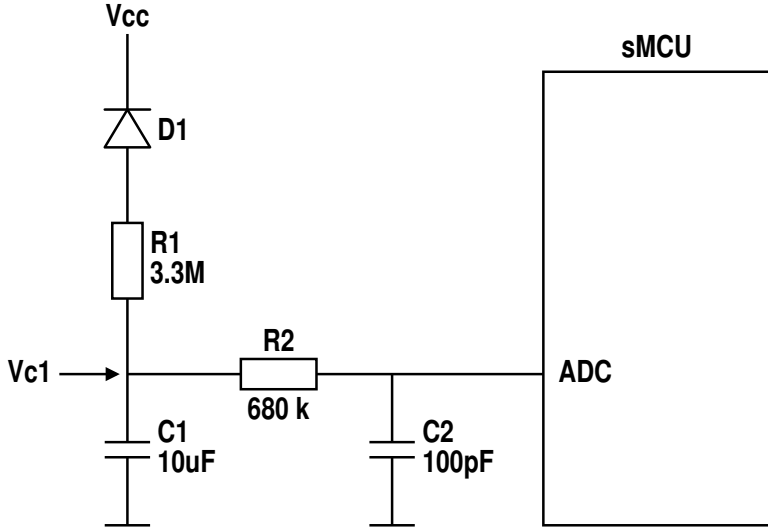


$V_{cc}$  = supply voltage (3.3 V)  
 $V_t$  = voltage at calibration point  
 $V_{min}$  =  $V_l$  goal, 90% of  $V_{cc}$  (?)  
 $V_h$  = measured high voltage  
 $V_l$  = measured low voltage  
 $V_s$  = measured/estimated start voltage  
 $V_s = f(V_h \text{ or } V_l, T_p, T)$   
 $V_e$  = measured end voltage

$T_t$  = calibration time  
 $T_d$  = discharge time,  $f(V_{cc}, V_{min}, T)$   
 $T_p$  = partial charge/discharge time  
 $T_{off}$  = calculated off time,  $f(V_s, V_e, T)$

$T$  = timing coefficient,  $f(V_t, T_t)$   
 (needs continuous recalibration)

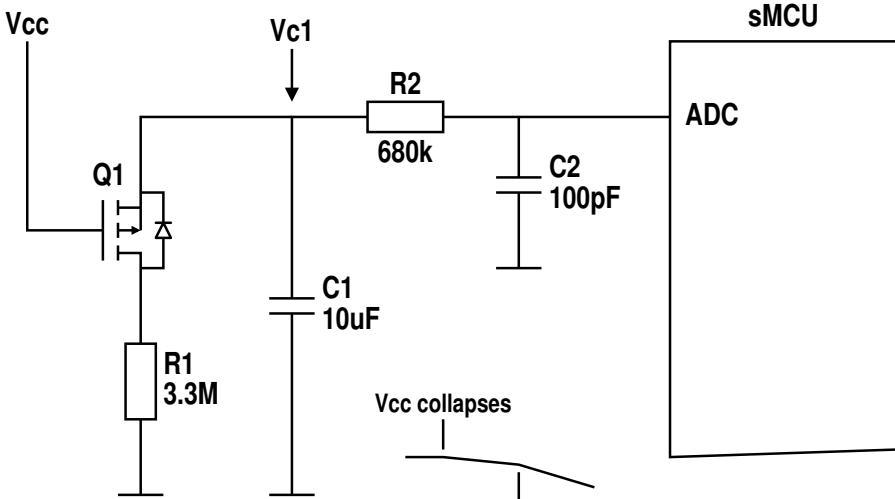
Based on design proposed by Joerg Reisenweber



**D1 prevents uncommanded charging**  
**C1, R1 control RC timing**  
**R2 protects C1 from GPIO upsets**  
**C2 filter, ADC buffer (optional)**

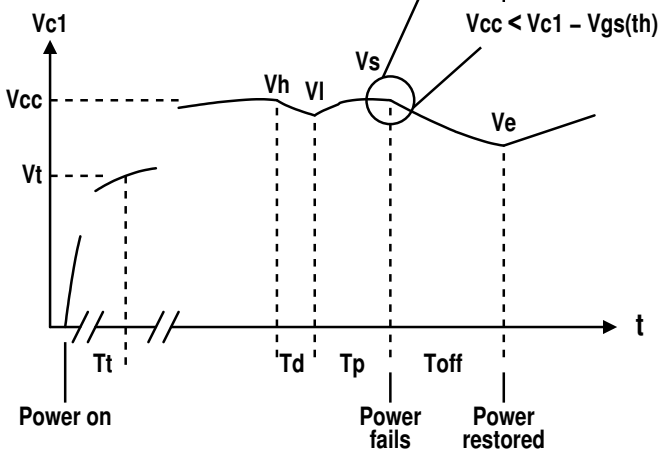
Phase	ADC
Discharge	L
Idle	H
Sample	ADC

Based on design proposed by Joerg Reisenweber



Q1 enables pull-down R1 when  $V_{cc} < V_{c1} - V_{gs(th)}$   
 C1, R1 control RC timing  
 C1, R1 control RC timing  
 R2 protects C1 from GPIO upsets  
 C2 filter, ADC buffer (optional)

Phase	ADC
Discharge	L
Idle	H
Sample	ADC



$V_{cc}$  = supply voltage (3.3 V)  
 $V_t$  = voltage at calibration point  
 $V_{min}$  =  $V_l$  goal, 90% of  $V_{cc}$  (?)  
 $V_h$  = measured high voltage  
 $V_l$  = measured low voltage  
 $V_s$  = measured/estimated start voltage  
 $V_s = f(V_h \text{ or } V_l, T_p, T)$   
 $V_e$  = measured end voltage

$T_t$  = calibration time  
 $T_d$  = discharge time,  $f(V_{cc}, V_{min}, T)$   
 $T_p$  = partial charge/discharge time  
 $T_{off}$  = calculated off time,  $f(V_s, V_e, T)$

$T$  = timing coefficient,  $f(V_t, T_t)$   
 (needs continuous recalibration)

Based on design proposed by Joerg Reisenweber